Midterm Exam

600.229 Computer Systems Fundamentals
Spring 2018
Johns Hopkins University
Instructor: Prof. Philipp Koehn

9 March 2018

Complete all questions.

Use additional paper if needed.

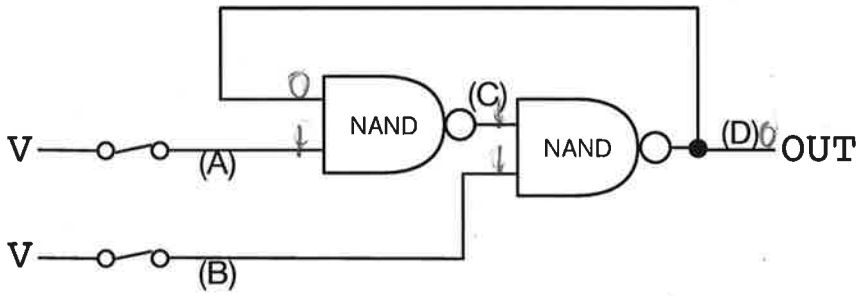
Time: 50 minutes.

Name of student:

Solution (corrected)

Q1. Analysis of Circuit *25 points*

Consider the following circuit:



Assume that at the onset, the wires are activated as follows: A=1, B=1, C=1, D=0.

Moreover, assume that it takes 1ms for a NAND gate to change its output value.

The following actions are performed:

- At time 10ms, the key connected to wire (B) is opened.
- At time 20ms, the key connected to wire (B) is closed.
- At time 30ms, the key connected to wire (A) is opened.
- At time 40ms, the key connected to wire (A) is closed.

Trace the activation levels for each wire (A)–(D) at each time step when wire activations change values.

Time	(A)	(B)	(C)	(D)
0 ms	1	1	1	0
10 ms	1	0	1	0
11 ms	1	0	1	1
12ms	1	0	0	1
20ms	1	1	0	1
30ms	0	1	0	1
31 ms	0	1	1	1
32ms	0	1	1	0
40ms	1	1	1	0

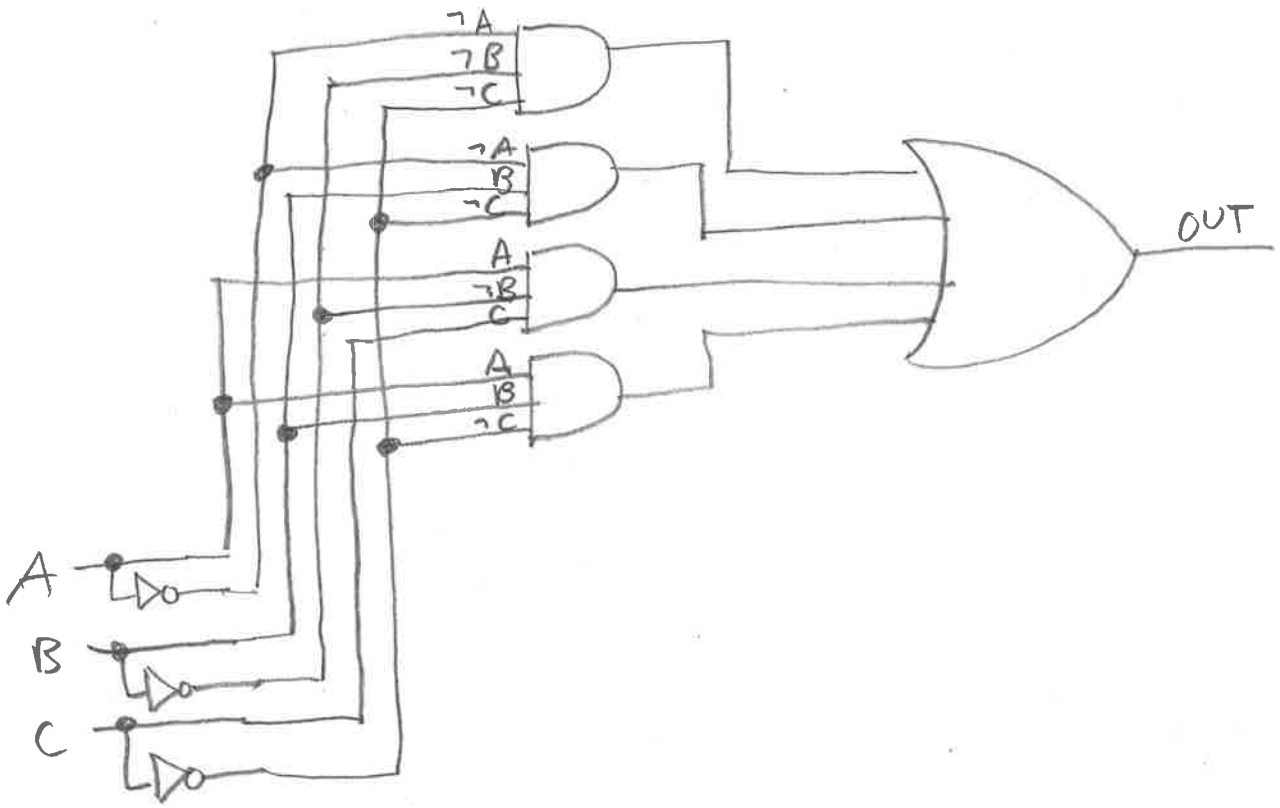
Q2. Design a Circuit

25 points

You are given the following truth table for a function.

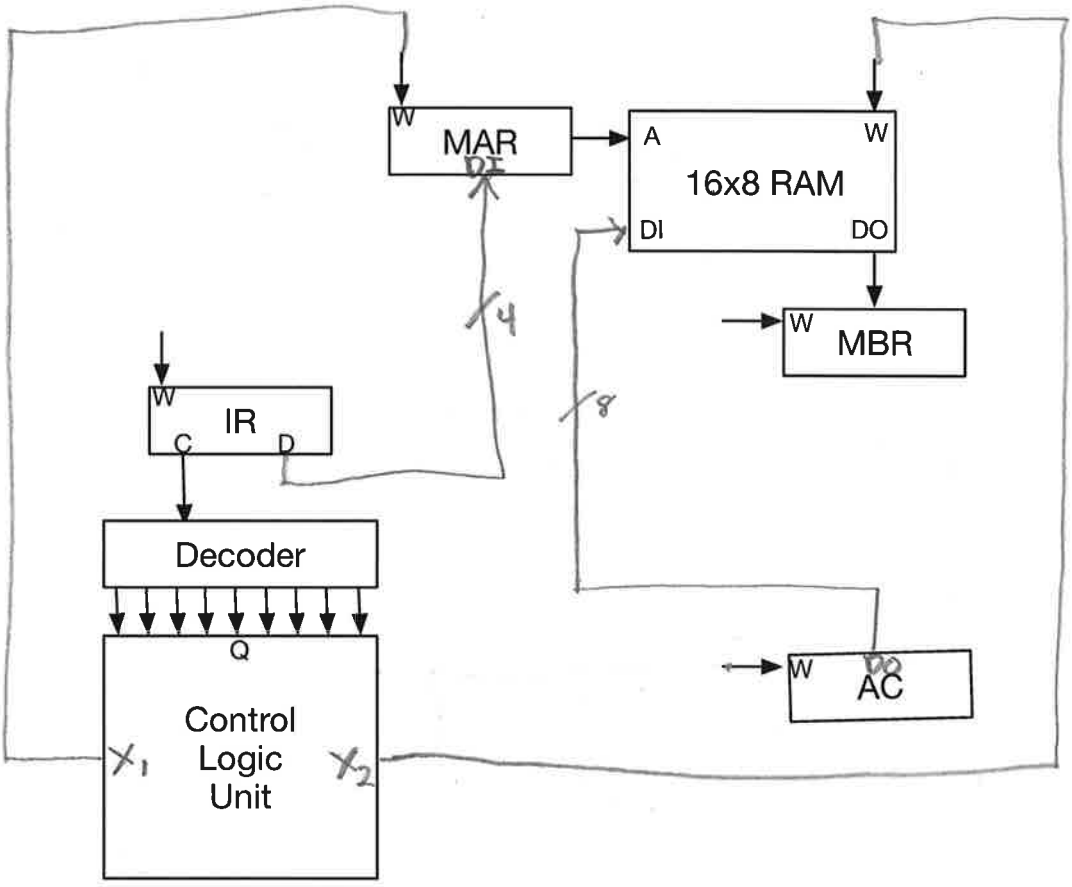
A	B	C	OUT
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Design a circuit with AND, OR, and NOT gates that implements this function (hint: use CNF or DNF).



Q3. SCRAM Circuit *25 points*

Below is an incomplete diagram of a SCRAM circuit (consisting of IR = Instruction Register, MAR = Memory Access Register, MBR = Memory Buffer Register, and AC = accumulator).



Design the STA command (storing a value from the accumulator into memory)

1. Add all the required control signal from the control logic unit and wiring to the diagram (you do not add anything inside the control logic unit).
2. Write the mirco-program that implements the STA command (you do not write micro-code for the instruction fetch).

control signal

Assume q_3 indicates STA

$t_3 q_3$: MAR ← IR(D) (X_1)

$t_4 q_3$: M ← AC; END (X_2)

$t_0 - t_2$ are steps for instruction fetch

reset timer to start instruction fetch for next instruction

Q4. SCRAM Code *25 points*

Consider the following code of a SCRAM-like program.

Address	Operation	Data
0	LDA	13
1	STA	14
2	DEC	13
3	JPZ	11
4	LDA	13
5	STA	15
6	LDA	14
7	DEC	15
8	JPZ	1
9	ADD	14
10	JMP	7
11	PRINT	14
12	HLT	
13	DAT	3
14	DAT	0
15	DAT	0

	Time	PC	M[13]	M[14]	M[15]	A
LDA	0	0	3	0	0	3
STA	1	1	3	3	0	3
DEC	2	2	2	3	0	3
JPZ	3	3	2	3	0	3
LDA	4	4	2	3	0	2
STA	5	5	2	3	2	2
LDA	6	6	2	3	2	3
DEC	7	7	2	3	1	3
JPZ	8	8	2	3	1	3
ADD	9	9	2	3	1	6
JMP	10	10	2	3	1	6
DEC	11	7	2	3	0	6
STA	12	1	2	6	0	6
DEC	13	2	1	6	0	6
JPZ	14	3	1	6	0	1
LDA	15	4	1	6	1	1
STA	16	5	1	6	1	6
LDA	17	6	1	6	0	6
DEC	18	7	1	6	0	6
JPZ	19	8	1	6	0	6
STA	20	1	1	6	0	6
DEC	21	2	0	6	0	6
JPZ	22	3	0	6	0	6
PRINT	23	11	0	6	0	6
HLT	24	12	0	6	0	6

prints: 6

Operations:

- STA: store accumulator
- LDA: load accumulator
- ADD: add to accumulator
- DEC: decrement the value at memory address
- JMP: jump to memory address
- JPZ: jump to memory address if last DEC resulted in 0
- DAT: dummy instruction (data value used only)
- PRINT: print value at memory address

What is the number printed by the program?
Show your work (for instance by reporting values in relevant memory locations).