Spartan3 Architecture

- Configurable Logic Blocks (CLBs)
  - RAM-based Look-Up Tables (LUTs) for logic
  - Storage elements configured as flip flops or latches

- Input/Output Blocks (IOBs)
  - Control data flow between I/O pins and internal logic
  - Various signal standards/terminations

- Block RAM
  - Data storage in 18k-bit dual-port blocks

- Multipliers
  - 2 18-bit binary inputs, 36 bit output

- Digital Clock Manager (DCM)
  - Distribute, multiply, divide, or shift clock
CLBs (4 Slices in a CLB)

From the Xilinx Spartan3 Datasheet
Slices

- 2 LUTs
  - 4 logic inputs, single output for any four-variable boolean logic operation
  - Can also function as ROM
  - “Left” slices can also be distributed RAM or 16-bit shift register
- 2 Storage elements
- 2 Multiplexers - to combine LUTs for more complex logic
- Carry logic, arithmetic gates - to support faster and more efficient math
A Left Slice

From the Xilinx Spartan3 Datasheet
Delay

- Pin delays
  - From pin to internal logic - a few ns

- Wire delays
  - Fast but still measurable
  - Some interconnects designed for local routing, some for distant

- Gate delays
  - From input of CLB to output of CLB
  - For our device, spec min=0.21ns, max=0.61ns
Flip flop timing

- **Setup** - Time data must be stable at input before clock edge (0.53ns)
- **Hold** - Time data must be stable at input after clock edge (0ns)
- **Clock-to-output** - Time from clock edge until data appears at output (min=0.24ns, max=0.72ns)
Fanout

- Number of lines driven by one signal
- As fanout increases, harder to drive lines
- Higher fanout means lower frequency signals
- Tools limit fanout by assigning signals to global clock networks, duplicating gates, or inserting buffers
- Designers can also control these tradeoffs
Adders

- **Half Adder**
  - Sum = A xor B
  - Carry Out = A and B

- **Full Adder**
  - Inputs: A, B, Carry In
  - Outputs: Sum, Carry Out

http://en.wikipedia.org/wiki/Adder_(electronics)
Making a multibit adder

- Adders are implemented in CLBs
- Takes advantage of the carry in, carry out lines
- Larger adders are still slower

http://www.aoki.ecei.tohoku.ac.jp/arith/mg/algorithn.html#fsa_rca